IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 19-22. These sheets, which include Figs. 19-22, replace the original sheets including Figs. 19-22.

Attachment: Replacement Sheets

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-22 are pending in this application.[1] Claims 1-22 were rejected under 35 U.S.C. §251. The figures were objected to. Claims 1-22 were rejected under 35 U.S.C. §112, second paragraph. Claims 1-4, 7-9, 12-15, and 18-20 were rejected under 35 U.S.C. §102(b) as anticipated by applicants' admitted art. Claims 5, 6, 10, 11, 16, 17, 21, and 22 were rejected under 35 U.S.C. §103(a) as unpatentable over applicants' admitted art.

Addressing first the rejection to claims 1-22 under 35 U.S.C. §251, that rejection is traversed by the present response.

The above-noted rejection is based on the position that the claim amendments previously submitted to recite the CVD nitride film not extending "beyond" an upper portion of said first gate was an improper amendment as the claims originally recited the CVD nitride film "not extending to an upper portion of said first gate" (emphasis added). To address that rejection each of independent claims 1 and 12 is amended to delete the term --beyond-- and to recite a CVD nitride film "not extending above an upper portion of said first gate". That amendment is believed to address the above-noted rejection, and the rejection noted in the Office Action of February 19, 2002, top of page 3.

Addressing now the objection to the drawings, replacement Figures 19-22 are submitted herein that are now labeled as --BACKGROUND ART--.

The drawings were also objected to as they were interpreted as having an inconsistency between Figures 1 and 8-12 with respect to the layer 16, which is not shown in Figure 7. In reply to that object applicants submit Figures 1 and 7 are proper and consistent. In that respect applicants point out Figure 1 shows a final formation and Figure 7 shows a

[1] The present response amends the claims and includes in the amendment to the claim Listing of Claims Section showing the amended claims relative to the original U.S. patent 5,945,692. An Appendix is also submitted showing the claim amendments relative to the previous pending claims, as submitted in the Response filed December 5, 2005.

manufacturing process. Applicants also point out the center layer 16 is removed so as to form impurity layer 5 at the center. After forming the impurity layer 5, the center layer 16 comes back when gate insulating film 7 is formed by thermal oxidation in the process of Figure 8. In that way the pattern layer 16 appears in the periphery of Figure 8.

In such ways, applicants respectfully submit the figures are consistent.

Addressing now the rejection of claims 1-22 under 35 U.S.C. §112, second paragraph, that rejection is traversed by the present response.

The above-noted rejections first ask for clarification of the positioning of the first semiconductor region, and particularly whether it is formed in the central portion or the peripheral portion. Each of claims 1 and 12 is now amended to clarify the positioning of the first semiconductor region.

Applicants also note the first semiconductor region (5) is formed selectively in the first major surface of the first semiconductor layer, and the first semiconductor region is formed selectively so that the first semiconductor layer remains along the peripheral portion of the first major surface, and the first semiconductor layer remains in a form of an insular region in a planar view in a central portion of the first major surface.

An embodiment of this configuration is shown in Figure 3; the first semiconductor layer (3) exists along the peripheral portion (30), and the first semiconductor region is formed in another part than the semiconductor layer (3).

In the central portion of the first major surface, which is the portion surrounded by the peripheral portion, the first semiconductor layer is formed in a form of an insular region in a planar view. Here, the first semiconductor region (5) is selectively formed in the other portion than the semiconductor layer (3) in an insular form and the second semiconductor region (6) by the side.

In view of the above comments, the positional relation of the first semiconductor region and the peripheral portion as now recited in claims 1 and 12 is clear.

In addition, Figure 3 shows that the first semiconductor layer is in a form of an insular region in a planar view surrounding by the peripheral.

The outstanding rejections under 35 U.S.C. §112, second paragraph also note the term "exposed" was unclear in the recited apparatus claims. In reply the claims are amended to no longer recite that term, and to clarify that language.

In view of the presently submitted amendments and foregoing comments, applicants respectfully submit each of the claims as currently written is proper under 35 U.S.C. §112, second paragraph.

Addressing the above-noted prior art rejections to each of claims 1-22 over applicants' admitted art, that rejection is traversed by the present response.

Applicants respectfully submit that no cited art, and particularly not the admitted art, discloses or suggests the claimed features that an integral semi-insulating plasma CVD nitride film does not extend above an upper portion of a first gate. With reference to Figure 2 in the present specification as a non-limiting example, the semi-insulating plasma CVD film 14 does not extend above an upper portion of the first gate 8.

The applicants of the present invention recognized in the background art such as shown for example in Figures 19 and 20 in the present specification that a structure is known in which a protective film 14 would extend above different gates 8. The applicants of the present invention recognized drawbacks for such a system, discussed throughout the "Description of the Background Art" section of the present application.

The applicants of the present invention in recognizing problems in the background art also recognized a solution to the problems, and particularly the solution being in limiting the extent of the CVD nitride film to not extend above an upper portion of the first gate. Without

recognizing the problems in the background art pointed out in the specification, one of ordinary skill in the art would clearly not have been led to any solution of such problems, and particularly would not have been led to a solution that limits the extent of the CVD nitride film such as in the claims as written.

The outstanding grounds for rejection is ignoring the fact that the admitted art does not even recognize any problems therein or any solution to such problems. The claimed invention recognized drawbacks in the admitted art and a specific solution of limiting the extent of a CVD nitride film to not extend above an upper portion of a first gate to solve such problems. Applicants submit such a structure is not disclosed in the admitted art and the admitted art does not achieve the benefits realized by the claimed structure.

Thereby, each of independent claims 1 and 12 as currently written is believed to positively recite a structure neither taught nor suggested by the admitted art of Figure 12. Thereby, each of claims 1-22 is believed to be allowable over the noted admitted art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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APPENDIX

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer ~~is exposed in~~ remains along a peripheral portion of said first major surface, and said first semiconductor layer ~~is exposed~~ remains in [[the]] a form of an insular region in a planar view in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a first gate formed on said gate insulating film and formed adjacent said peripheral portion;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and

not extending ~~beyond~~ above an upper portion of said first gate, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

2. (Original) The semiconductor device of claim 1, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

3. (Previously Presented) The semiconductor device of claim 1, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

4. (Original) The semiconductor device of claim 3, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

5. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

6. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

7. (Original) The semiconductor device of claim 1, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

8. (Previously Presented) The semiconductor device of claim 7, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected.

9. (Previously Presented) The semiconductor device of claim 8, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

10. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

11. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

12. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer ~~is exposed in~~ remains along a peripheral portion of said first major surface, and said first semiconductor layer ~~is exposed~~ remains in [[the]] a form of a plurality of insular regions in a planar view in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a first gate formed on said gate insulating film and formed adjacent said peripheral portion;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending ~~beyond~~ to an upper portion of said first gate, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

13. (Original) The semiconductor device of claim 12, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

14. (Previously Presented) The semiconductor device of claim 13, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

15. (Original) The semiconductor device of claim 14, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

16. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

17. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

18. (Original) The semiconductor device of claim 13, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

19. (Previously Presented) The semiconductor device of claim 18, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

20. (Original) The semiconductor device of claim 19, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

21. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

22. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).